What is claimed is:

1. A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a plurality of conductive patterns on a substrate in a cell region and a peripheral circuit region;

(b) forming an insulation layer on an entire surface of the resulting structure from the step (a);

(c) forming a plurality of plugs in the cell region and simultaneously forming a dummy pattern in a region between the cell region and the peripheral circuit region, each plug and the dummy pattern being contacted to the substrate allocated between the conductive patterns by passing through the insulation layer;

(d) forming a photoresist pattern masking the resulting structure in the cell region; and

(e) removing the insulation layer in the peripheral circuit region by performing a wet etching process with use of the photoresist pattern as an etch mask to thereby expose a surface of the substrate in the peripheral circuit region.

2. The method as recited in claim 1, wherein the region for the dummy pattern has a width ranging from about 1 μm to about 10 μm.

3. The method as recited in claim 1, wherein the insulation layer is made of any material selected from a group

consisting of boron-phosphorous silicate glass (BPSG), high density plasma (HDP) oxide or tetra-ethyl-ortho silicate (TEOS) glass.

4. The method as recited in claim 1, wherein the conductive pattern is a gate electrode pattern.

5. The method as recited in claim 1, wherein the wet etching process uses buffered oxide etchant (BOE) or hydrofluoric acid (HF).

6. A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a plurality of conductive patterns on a substrate in a cell region and a peripheral circuit region;

(b) forming an insulation layer on an entire surface of the resulting structure from the step (a);

(c) forming a plurality of plugs in the cell region, each being contacted to the substrate allocated between the conductive patterns by passing through the insulation layer;

(d) forming a photoresist pattern masking the resulting structure in the cell region;

(e) performing a dry etching process with use of the photoresist pattern as an etch mask to remove partially the insulation layer in the peripheral circuit region; and

(f) removing the remaining insulation layer through a wet etching process to thereby expose a surface of the

substrate in the peripheral circuit region.

7. The method as recited in claim 6, wherein the conductive pattern is a gate electrode pattern.

8. The method as recited in claim 6, wherein a plasma using a mixed gas of C_xF_y, where x and y ranges from about 1 to about 10, $C_aH_bF_c$, where a, b and c ranges from about 1 to about 10, and O2 is used in the dry etching process.

9. The method as recited in claim 6, wherein the insulation layer is made of any material selected from a group consisting of boron-phosphorous silicate glass (BPSG), boron-silicate glass (BSG), phosphorus-silicate glass (PSG), high density plasma (HDP) oxide, tetra-ethyl-ortho silicate (TEOS) glass or advanced planarization layer (APL).

10. The method as recited in claim 6, wherein the dry etching process uses additionally an inert gas.

11. The method as recited in claim 6, wherein the wet etching process uses buffered oxide etchant (BOE) or hydrofluoric acid (HF).

12. A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a plurality of conductive patterns on a

substrate in a cell region and a peripheral circuit region;

(b) forming a planarized first insulation layer on an entire surface of the resulting structure from the step (a);

(c) forming a second insulation layer on the first insulation layer;

(d) forming a plurality of plugs in the cell region, each being contacted to the substrate allocated between the conductive patterns by passing through the first and the second insulation layers;

(e) forming a photoresist pattern masking the resulting structure in the cell region; and

(f) performing a wet etching process with use of the photoresist pattern as an etch mask to remove the first and the second insulation layers disposed in the peripheral circuit region.

13. The method as recited in claim 12, wherein the first insulation layer is made of BPSG and the second insulation layer is made of TEOS or HDP oxide.

14. The method as recited in claim 12, wherein the conductive pattern is a gate electrode pattern.

15. The method as recited in claim 12, wherein the wet etching process uses a buffered oxide etchant (BOE) or hydrofluoric acid (HF).